Amendments to the Specification

Please replace the paragraph beginning at page 10, line 8, with the following rewritten paragraph:

FIGS. 3A-3B show the substrate assembly 217 prior to etching. The substrate assembly 217 may be a silicon wafer 217b covered with a silicon oxide layer 217a. The silicon wafer 217b typically has a thickness of less than 1-2 mm and a diameter of 50-600 mm and can be doped or undoped. The silicon oxide layer 217a can be formed in different ways such as, for example, deposited from a gas such as tetraethyoxysilane (TEOS) or thermally grown (thermal oxide). The oxide layer 217a is coated with a patterned resist layer 301, the resist layer having a nominal thickness t_N. Apertures 303, 305 are provided in the resist layer 301 to permit substrate etching. Although fabrication processes attempt to maintain planarity of the substrate assembly 217, the substrate assembly 217 generally has one or more high regions such as the region 307. At the region 307, the thickness of the resist layer 301 is less than the nominal thickness t_N. When situated on the substrate assembly chuck 211, the oxide layer 217a and the resist layer 301 are exposed to the plasma in the chamber 203. The resist layer 301 can be made of any suitable resist material, including photoresists, deep ultraviolet resists, X-ray resists, electron beam resists, I-line resists, and multilayer resists. The selected resist material can be deposited by spin coating or any other suitable method, and patterned with conventional photolithographic or other patterning process, such as X-ray, I-line, and electron beam lithography.